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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MURALIDAR, RICHARD V	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,275	LIPCSEI ET AL.	
	Examiner	Art Unit	
	Richard V. Muralidar	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 and 13-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Wei [U.S. 2004/0100805].

With respect to Claims 1 and 6, **[amended]** Wei discloses a power converter [Fig. 2, par. 0005 lines 1-5, microprocessor with a power converter], said power converter comprising: a transformer [Fig. 2, transformer M] having a primary winding and a secondary winding [Fig. 2, transformer M with primary winding W1, secondary winding W2]; and a plurality of switches coupled to said primary and secondary winding [Fig. 2 switches Q1-Q6], said plurality of switches responsive to at least one control signal to short both said primary and secondary winding during a first reset time interval [page 2, par. 0023; Fig. 4C shows switches Q2 and Q3 operable to short both primary and secondary of transformer M], said plurality of switches includes a first pair of switches [Fig. 2, the first pair of switches is Q1 and Q2] configured to be simultaneously controlled using a first control signal [Fig. 5, switches Q1 and Q2 are shown controlled by the same signal over one full cycle] and a second pair of switches

[Fig. 2, switches Q3 and Q4] configured to be simultaneously controlled using a second control signal [Fig. 5, switches Q3 and Q4 are shown controlled by the same signal over one full cycle], wherein the first pair of switches is coupled in series [Fig. 2, switches Q1 and Q2 are coupled in series through primary winding W1 and capacitor C1] to one end of said secondary winding [Fig. 2, switch Q2 is coupled to the top end of secondary winding w2] and the second pair of switches is coupled in series [Fig. 2, switches Q3 and Q4 are coupled in series through primary winding W1 and capacitor C1] to an opposite end of said secondary winging [Fig. 2, switch Q3 is coupled to the bottom end of secondary winding w2].

With respect to Claims 2 and 7, [original] Wei discloses that said plurality of switches comprises: a first high side switch [Fig. 2 switch Q1] and a first low side switch [Fig. 2 switch Q3] coupled in series along a first path [Fig. 2 path 22] of a full bridge circuit [Fig. 2 switches Q1-Q4], a first node between said first high side switch and said first low side switch [Fig. 2 node 24]; and a second high side switch [Fig. 2 switch Q4] and a second low side switch [Fig. 2 switch Q2] coupled in series along a second path [Fig. 2 path 20] of said full bridge circuit, a second node [Fig. 2 node 24] between said second high side switch and said second low side switch, wherein said primary winding [Fig. 2 primary W1] is coupled between said first node and said second node, and wherein said first and second high side switches [Q1 and Q4] are adapted to open and said first and second low side switches [Q2 and Q3] are adapted to close during said first reset time interval to short said primary winding [Fig. 4C free wheeling mode].

With respect to Claims 3 and 8, [original] Wei discloses that said plurality of switches further comprises: a first rectifier switch coupled to one end of said secondary winding [Fig. 2 switch Q5]; and a second rectifier switch coupled to an opposite end of said secondary winding [Fig. 2 switch Q6], wherein said first and second rectifier switches are adapted to close during said first reset time interval to short said secondary winding [Fig. 4A and 4C free wheeling mode show the rectifier switches shorting the secondary to ground].

With respect to Claims 4 and 9, [original] Wei discloses that said first low side switch [Q2] of said first path of said full bridge circuit and said first rectifier switch [Q5] are responsive to a first control signal and said second low side switch [Q3] of said second path of said full bridge circuit and said second rectifier switch [Q6] are responsive to a second control signal [the configurations in Fig 4C, 7A and 7C show that Q2 and Q5 are synchronized, and Q3 and Q6 are synchronized].

With respect to Claims 5 and 10, [original] Wei discloses that said first high side switch [Q4] of said first path of said full bridge circuit is responsive to a third control signal and said second high side switch [Q1] of said second path of said full bridge circuit is responsive to a fourth control signal [Figs. 4A, 4C, 7A and 7C show switches Q4 and Q1 synchronized].

With respect to Claim 11, [currently cancelled] Wei discloses a method comprising: sampling an input voltage onto a primary winding of a transformer during a first time interval; and shorting said primary winding of said transformer during a second time interval [Fig. 4C encompasses this method].

With respect to Claim 12, [currently cancelled] Wei discloses a method shorting a secondary winding of said transformer during said second time interval [Fig. 4A encompasses this method].

With respect to Claim 13, [original] Wei discloses a method comprising: providing a first control signal [Fig. 3 control signal Q4] to control a state of a first high side switch [Fig. 2 Q4] coupled to a first path of a full bridge circuit [Fig. 2 switches Q1-Q4]; providing a second control signal [Fig. 3 control signal Q1] to control a state of a second high side switch [Fig. 2 Q1] coupled to a second path of said full bridge circuit, said full bridge circuit coupled across a primary winding of a transformer [Fig. 2 primary winding W1]; providing a third control signal to simultaneously control [Figs. 4C and 7C show Q2 and Q5 operating simultaneously] a state of a first low side switch [Fig. 2 Q2] coupled to said first path of said full bridge circuit and a state of a first rectifier switch of a rectifier circuit [Fig. 2 Q5], said first rectifier switch coupled to one end of a secondary winding of said transformer [Fig. 2 secondary winding W2]; and providing a fourth control signal to simultaneously control [Figs. 4C and 7C show Q3 and Q6 operating simultaneously] a state of a second low side switch [Fig. 2 Q3] coupled to said second path of said full bridge circuit and a state of a second rectifier switch [Fig. 2 Q6] of said rectifier circuit, said second rectifier switch coupled to an opposite end of said secondary winding of said transformer.

With respect to Claim 14, [original] Wei discloses a method comprising: shorting said primary winding [Fig. 2 secondary W1] during a first time interval by closing said first low side switch [Fig. 2 Q2] of said first path of said full bridge circuit and by closing

said second low side switch [Fig. 2 Q3] of said second path of said full bridge circuit during said first time interval [Fig. 4C and 7C show Q2 and Q3 shorting the primary of the transformer].

With respect to Claim 15, [original] Wei discloses a method comprising: shorting said secondary winding [Fig. 2 primary W1] during said first time interval by closing said first rectifier switch [Fig. 2 Q5] and by closing said second rectifier switch [Fig. 2 Q6] during said first time interval [Fig. 4A and 4C show Q5 and Q6 shorting the secondary of the transformer].

With respect to Claim 16, [**amended**] Wei discloses a power converter [Fig. 2, par. 0005 lines 1-5, microprocessor with a power converter] comprising: a full bridge circuit [Fig. 2 switches Q1-Q4 are arranged in a full bridge; par. 0023 lines 1-3] having a first path [Fig. 2 path 20] and a second path [Fig. 2 path 22], each path comprising a high side [Fig. 2 switch Q4] and low side bridge switch [Fig. 2 switch Q2] coupled in series, each path having a node [Fig. 2, node 24] between said high side and low side bridge switches, and each path coupled to an input voltage terminal [Fig. 2, first and second paths are coupled to Vin]; a transformer [Fig. 2, transformer M] having a primary winding [Fig. 2, primary winding W1] and a secondary winding [Fig. 2, secondary winding W2], said primary winding being coupled between said nodes of said paths of said full bridge circuit [the primary winding W1 is shown coupled between the upper and lower nodes 24]; and a rectifier circuit coupled to said secondary winding [Fig. 2, transistors Q5 and Q6 are the rectifiers of this buck converter], said rectifier circuit comprising a first [Fig. 2, transistor Q5] and second rectifier switch [Fig. 2 switch

Q6], said first rectifier switch coupled in series to said low side switch [Fig. 2, switch Q5 is coupled to switch Q2] of said first path and to one end of said secondary winding [Fig. 2, the top end of secondary winding W2], said second rectifier switch coupled in series to said low side switch [Fig. 2, switch Q6 is coupled to switch Q3] of said second path and to an opposite end of said secondary winding [Fig. 2, the top end of secondary winding W2], said low side switch [Q2] of said first path [20] and said first rectifier switch [Q5] simultaneously driven by a first control signal [Fig. 4C and 7C show Q2 and Q5 simultaneously controlled ON] and said low side switch [Q3] of said second path [22] and said second rectifier switch [Q6] simultaneously driven by a second control signal [Fig. 4C and 7C show Q3 and Q6 simultaneously controlled ON, at least of a portion of the switching cycle- Fig. 3. Additionally, Wei's circuit contains identical hardware components as applicant's circuit and is fully capable of being operated with 4 signals given the proper controller and fine-tuning for resonance effects].

With respect to Claim 17, [original] Wei discloses that high side switches [Fig. 2 Q1 and Q4] of said first and second paths are adapted to open [Fig. 4C show them opened] and said low side switches [Fig. 2, Q2 and Q3] of said first and second paths are adapted to close [Fig. 4C show them closed] during a reset time interval to short said primary winding [Fig. 4C shows primary winding W1 shorted to secondary winding W2].

With respect to Claim 18, [original] Wei discloses that said first and second rectifier switches [Fig. 2, Q5 and Q6] are also adapted to close during said first reset time interval to short said secondary winding during said reset time interval [Fig. 4C

show Q5 and Q6 closed, in conjunction with Q2 and Q3 closed, and Q1 and Q4 opened].

With respect to Claim 19, [**amended**] Wei discloses a power converter comprising a plurality of DC to DC converters coupled in parallel [page 4 par. 0053; Fig. 8], at least one of said plurality of DC to DC converters [Fig. 8 converters 28, 30, 32, 34] comprising: a transformer [M1] having a primary winding and a secondary winding [W1 and W2]; and a plurality of switches coupled to said primary and second winding [switches Q1-Q8], said plurality of switches responsive to at least one control signal to short both said primary and secondary winding during a first reset time interval [Fig. 8 is the plural "multi-output" version of Fig. 2, with multiple, parallel output converters connected to the secondary, therefore the primary and secondary are shorted in the same manner], said plurality of switches includes a first pair of switches [Fig. 2, the first pair of switches is Q1 and Q2] configured to be simultaneously controlled using a first control signal [Fig. 5, switches Q1 and Q2 are shown controlled by the same signal over one full cycle] and a second pair of switches [Fig. 2, switches Q3 and Q4] configured to be simultaneously controlled using a second control signal [Fig. 5, switches Q3 and Q4 are shown controlled by the same signal over one full cycle], wherein the first pair of switches is coupled in series [Fig. 2, switches Q1 and Q2 are coupled in series through primary winding W1 and capacitor C1] to one end of said secondary winding [Fig. 2, switch Q2 is coupled to the top end of secondary winding w2] and the second pair of switches is coupled in series [Fig. 2, switches Q3 and Q4 are coupled in series through primary winding W1 and capacitor C1] to an

opposite end of said secondary winging [Fig. 2, switch Q3 is coupled to the bottom end of secondary winding w2].

With respect to Claim 20, [original] Wei discloses that said plurality of switches comprises: a first high side switch and a first low side switch coupled in series along a first path of a full bridge circuit, a first node between said first high side switch and said first low side switch; and a second high side switch and a second low side switch coupled in series along a second path of said full bridge circuit, a second node between said second high side switch and said second low side switch, wherein said primary winding is coupled between said first node and said second node, and wherein said first and second high side switches are adapted to open and said first and second low side switches are adapted to close during said first reset time interval to short said primary winding [Fig. 8 is the plural "multi-output" version of Fig. 2, with multiple, parallel output converters connected to the secondary. Therefore the first and second high side switches and first and second low side switches respectively open and close in exactly the same manner as described for Fig. 2 for the previous claims].

With respect to Claim 21, [original] Wei discloses that said plurality of switches further comprises: a first rectifier switch coupled to one end of said secondary winding; and a second rectifier switch coupled to an opposite end of said secondary winding, wherein said first and second rectifier switches are adapted to close during said first reset time interval to short said secondary winding [Fig. 8 is the plural version of Fig. 2, with multiple, parallel output converters connected to the secondary. Therefore the first

and second rectifier switches close to short the secondary winding in exactly the same manner as described for Fig. 2 for the previous claims].

With respect to Claim 22, [original] Wei discloses that said plurality of switches for each said DC to DC converter are responsive to control signals from a driver associated with each said DC to DC converter [page 2 par. 0026].

With respect to Claim 23, [original] Wei discloses that said plurality of switches comprise MOSFET transistors [page 2, par. 0026 states Q1-Q6 are FETs; the most popular ones are known to be MOSFETs] and said driver comprises a dual MOSFET driver [page 2, par. 0026, the driving circuit is well known in the art, and the MOSFET driver/ dual driver is widely used to drive MOSFETs].

RESPONSE TO ARGUMENTS

Applicant's arguments filed 03/29/2006 have been fully considered but they are not persuasive, for the following reasons:

Applicant's main (and only) argument as disclosed on pages 14 and 15 of applicant's REMARKS states that switches Q5 and Q2 (i.e. the first rectifier switch and the first low side switch) are not simultaneously controlled using a first control signal, and switches (Q6 and Q3) (i.e. the second rectifier switch and the second low side switch) are not simultaneously controlled using a second control signal. Applicant points out that his invention effectively controls 6 switches with 4 control signals, by combining the switching signals of two pairs of two switches [Q2 with Q5 and Q3 with Q6], whereas Wei requires 6 control signals to control all each of the 6 switches.

After careful comparison of Wei's circuit [Fig. 2] to applicant's circuit [Fig. 2], examiner has concluded that there is a difference only in the switching signals of the two circuits; *and that this difference is so small that it does not constitute new, patentable material.* Structurally, the two circuits are identical: both circuits are converters employing 6 switches. Two pairs of switches form a high side and two pairs of switches form a low side, connected across a non-isolated transformer as described. The final pair of switches forms a rectifier for creating a dc output. Vin is inputted across the two pairs of switches, and Vout is taken across a grounded capacitor. Both circuits switch transistors Q1 with Q2, and Q3 with Q4, with identical control signals, respectively [see Wei, Fig. 5].

The minor difference arises in the switching of rectifier Q5 with switch Q2, and rectifier Q6 with switch Q3, respectively. Wei discloses that these switches are switched simultaneously during *a portion of 1 full cycle*, as opposed to the *entire* cycle [see Fig. 3, comparing the signals of Q2 to Q5 and Q3 to Q6], as applicant's invention discloses. This difference is reflected in applicant's claim language in claim 16, which reads: *"...said first rectifier switch simultaneously driven by a first control signal and said low side switch of said second path and said second rectifier switch simultaneously driven by a second control signal..."* Wei's switching scheme shown in Fig. 3 which shows simultaneous switching for a portion of the cycle, is sufficient to meet the first part of this claim language, and applicant's corresponding argument. The second part of the claim language that reads *"driven by a second control signal"* reflects that applicant has merely combined two signals into one, as discussed above, and tuned the circuit to

work with 4 control signals instead of 6 control signals. However, Wei's circuit is fully capable of being operated with 4 control signals [since the hardware is identical] given the proper controller and fine-tuning of circuit values (resistance, capacitance etc.).

Finally [and most significantly], applicant's claim language/invention is directed towards the actual *power converter circuit*, which has been fully met by Wei (i.e. Wei's circuit is fully capable of being operated with 4 signals given the proper controller and fine tuning for resonance effects). Applicant's claim language and invention are NOT directed towards a *controller* for a power converter circuit, with internal hardware and software as necessary to output 4 controller signals, with feedback to monitor output etc.

Applicant's arguments have been fully considered and rebutted. Applicant's amended claims have been considered, and the rejection under 35 U.S.C 102(e) in view of Wei [U.S. 2004/0100805] stands. Accordingly:

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

The following reference is cited for its disclosure of a non-isolated bridge buck DC-DC converter with self-driven synchronous rectifiers. Prior art [US2004/0246748A1] by Xu is cited for the disclosure of a similar arrangement of transistors to short-circuit the primary and secondary windings of a transformer to ground.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard V. Muralidar whose telephone number is 571-272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/26/2006
RVM

KARL EASTHOM
SUPERVISORY PATENT EXAMINER